Veriest

EE Thesis Projects at Veriest

Veriest is an international ASIC and FPGA design house, providing advanced design, verification solutions and IPs. We serve leading clients in industries such as networking, data communications, consumer electronics and wireless communications, applying our innovative methodologies and proven expertise to provide our customers with an unsurpassed competitive edge.

Veriest is based in Tel Aviv, Israel, and in Savograd, New Belgrade. We are inviting EE students to complete their thesis on-board, while acquiring the professional skill and training required for a promising future in verification.

Complete your thesis in a dynamic international environment, and attain a groundbreaking profession in today's technological frontier.

For more on Veriest thesis projects and requirements,

Contact us by mail office-bg@veriest-v.com or by phone: +381.11.6149.302

Veriest thesis projects are based on acquiring advanced verification knowledge, by constructing verification environments using standard industry protocols.

Students writing their thesis at Veriest will receive intensive in-house training in verification methodologies and languages (Specman or SV), will acquire basic knowledge of Verilog HDL, and will get to know related protocols.

Veriest offers several different thesis scopes to choose from, depending on the student's skill and selected protocol complexity.

Each thesis will be written on-site, at the Veriest offices, Savograd, New Belgrade.

Based on thesis excellence, Veriest will be honored to offer EE graduates an opportunity to stay on-board and join its international team of verification leaders

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