HDL Design House
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HDL Design is chip design/verification company located in Serbia and has two design centers with more than 60 engineers. HDL Design House offers front/back end design and verification services for SoC projects, analog design services, software development, providing soft IP cores and verification IP (VIP).

As a member of our team you will have the chance to work on the most demanding projects for leading semiconductor companies in industry.

As a top company in a fast growing industry, we have a great working environment where engineering is our top priority. We manage to keep a vibrant, startup-like environment where innovation and technology advancement occur on a daily basis. You will have the chance to shine as a top contributor and rise in the ranks of a growing company while working in an exciting, technology space.

HDL Design House is continuously expanding its digital and verification IC design teams with junior, senior designers and team leaders.

We are seeking for :

Senior Verification Designer - 5 positions

The ideal candidate will have following skills and background:

- Graduate Computer Science/Electronics
- Good communication skills and ability to succinctly describe design implementations as well as system challenges
- Candidate must have an open mind and an unparalleled ability to learn a new design and new verification methodologies.
- Minimum 3 + years of experience in verification domain,
- SystemVerilog/OVM/UVM and "e" (Specman) languages
- Must be proficient with OOP (C++, Java)
- Knowledge of Digital Integrated Circuits
- Knowledge of Hardware Description Languages (VHDL/Verilog)
- Proficient Unix user
- Fluent English is a must

Following skills will be a plus:

- Knowledge of AMBA AHB/AXI, OCP, PCI Express, Ethernet interfaces
- Experience of Verilog, VHDL and scripting languages
- Familiar with scripting tools and languages (e.g. bash, csh, awk, Perl)
- Familiar with development tools (e.g. make and versioning tools (e.g. CVS)

Responsibilities:

- Implement complete verification solutions using advanced verification methodologies
- Develop or maintain ASIC verification environments to support ASIC development

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- Responsible for development and deployment of coverage driven verification methodology
- Responsible for development of SystemVerilog/UVM VIP, constrained random verification environment, test plans and regressions
- Planning and execution of block and system level verification
- Working with design team in all the phases of the verification process to meet quality requirements at block and system level
- Required to use assertions, simulations and debugging on daily basis
- Should be able to comprehend the 'big picture' at the architectural level as well as execute at the detail implementation level
- Proactively collaborate with team members in different locations

Apply by sending your CV to: jobs@hdl-dh.com