EE Thesis Projects at Veriest Venture

Veriest Venture is an international IC and FPGA design house, providing advanced design, verification solutions and IPs. We serve leading clients in industries such as networking, data communications, consumer electronics and wireless communications, applying our innovative methodologies and proven expertise to provide our customers with an unsurpassed competitive edge.
Based in Tel Aviv, Israel, Veriest Venture has opened a subsidiary in Savograd, New Belgrade, inviting EE students to complete their thesis on-board, while acquiring the professional skill and training required for a promising future in verification.

Complete your thesis in a dynamic international environment, and attain a groundbreaking profession in today's technological frontier.

For more on Veriest thesis projects and requirements, contact Prof. Jelena Popovic-Bozovic at: jelena@etf.rs

Veriest Venture thesis projects are based on acquiring advanced verification knowledge, by constructing verification environments using standard industry protocols.
Students writing their thesis at Veriest Venture will receive intensive in-house training in verification methodologies and languages (Specman or SV VMM), will acquire basic knowledge of Verilog HDL, and will get to know related protocols.
All thesis projects described below can be implemented in Specman or System Verilog VMM, the industry standard verification languages.
Veriest Venture offers several different thesis scopes to choose from, depending on the student's skill and selected protocol complexity.
All thesis projects can serve as stand-alone verification components, or be incorporated into the Veriest IP portfolio family.

Each thesis will be written on-site, at the Veriest offices, Savograd, New Belgrade.

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Based on thesis excellence, Veriest Venture will be honored to offer EE graduates an opportunity to stay on-board and join its international team of verification leaders.

Verification IP technology

All projects include development of Verification IPs (VIPs).
A Verification IP is a software package that is capable of driving a standard bus or interface in order to verify a digital design module. The VIP is used in a verification environment to drive the bus, monitor the transactions on the bus and perform protocol checking. This way, the RTL design standard compliancy is verified.
Each VIP can be designed as a Slave or a Master. A Slave VIP is used to verify a Master RTL and vise versa

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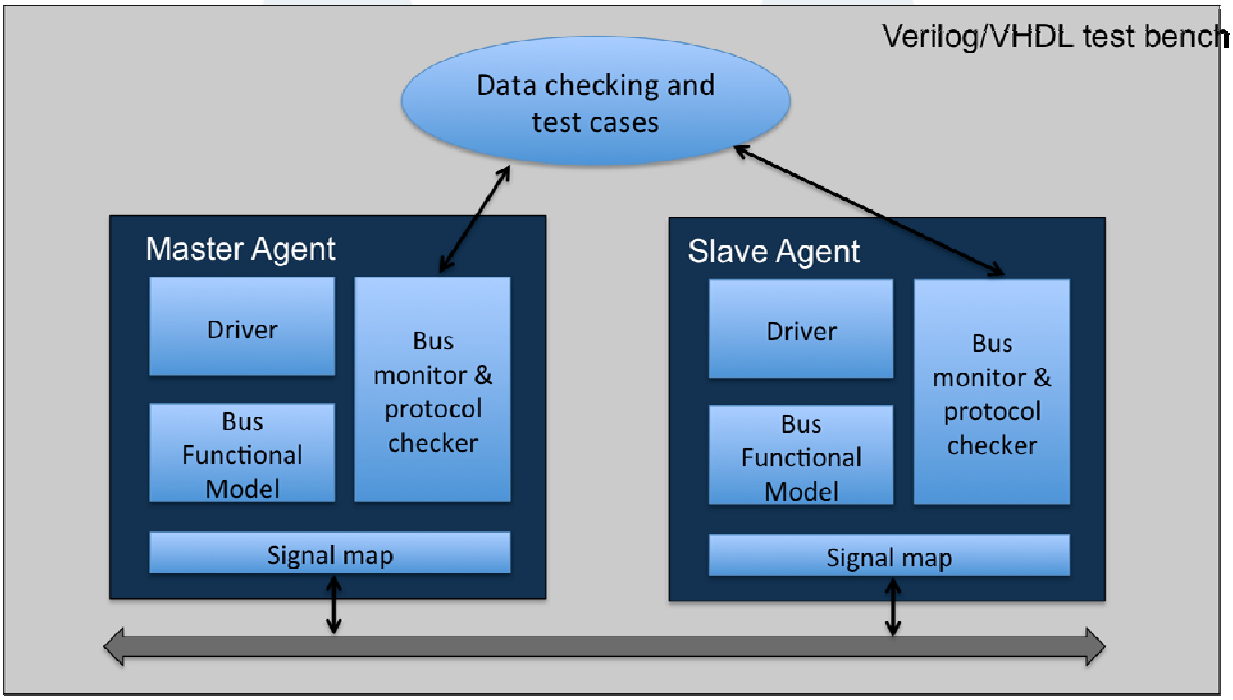
VIP architecture

The VIP architecture is Cadence eRM standard compliant or Synopsys VMM standard compliant. All VIPs have a common architecture while the internal components are specific per protocol. This is an industry standard that enables fast ramp up on a new protocol.

A diagram of the VIP is presented below.



Project description and stages:

1. Specman or SystemVerilog verification training.
2. eRM/VMM methodology training.
3. Learning the protocol specification Spec.
4. Defining the architecture of the VIP. Creating an architecture document.
5. Specman-eRM or SystemVerilog-VMM based VIP implementation.
6. VIP functional coverage definitions and testing.

Acceptance criteria:

1. Review of the VIP architecture by Hagai Arbel, Veriest's CEO.
2. Passing eRM/VMM compliance tests.
3. Passing the protocol compliance tests.

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4. Complete test suite with 100% coverage.
5. Code review by Veriest's Verification experts.

Proposed projects for thesis:

All projects:

- **Include the above stages and acceptance criteria.**
- **Can be implemented in Specman or System Verilog.**

Project No. 1
Development of Tensilica CPU PIF bus Verification IP:
Protocol: PIF lite standard.
Estimated effort: 3 month for two students.
Can be divided for two students: One will develop the slave side and the other will develop the master side.

Project No. 2
Development of AMBA AHB lite CPU bus Verification IP:
Protocol: AMBA3 AHB lite.
Estimated effort: 3 month for two students.
Can be divided for two students: One will develop the slave side and the other will develop the master side.

Project No. 3
Development of AMBA APB3 compliance Verification IP:
Protocol: AMBA APB3 standard.
Estimated effort: 2 month.

Project No. 4
Development of SPI flash memory bus Master VIP:
Protocol: SPI 2.0 standard.
Estimated effort: 3 month.

Project No. 5
Development of SPI flash memory bus Slave VIP:
Protocol: SPI 2.0 standard.

Estimated effort: 2 month.

Project No. 6
Development of Ethernet 802.3 VIP - Layer 2:
Protocol: IEEE 802.3 standard.
Estimated effort: 3.5 month.

Project No. 7
Development of Ethernet 802.3 VIP - Layers 2-4:
Protocol: IEEE 802.3 standard.
Estimated effort: 3.5 month.

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