On Computing Error Floor LDPC Codes

Abstract:

Computing error floors of low-density parity check (LDPC) codes is numerically challenging task especially when low frame error rates (FER) of 1e-12 or below are required. We present a computationally efficient, accurate and generic method for FER computation for LDPC codes over the binary symmetric channel (BSC). The sub-graph Expansion-Contraction method 1). starts from a list of short cycles present in the Tanner graph of a code, 2). expands each cycle by including its sufficiently large neighborhood in the Tanner graph and then, 3). contracts them based on exhaustive decoding of error patterns on the expanded graph. The method gives minimal uncorrectable error patterns, their corresponding strengths and thereby an estimation of the frame error rate. Computational complexity in estimating error floor of LDPC decoder is reduced six orders of magnitude compared with standard Monte-Carlo simulations.

Biography of Bane Vasic:

Dr. Bane Vasic is a Professor of Electrical and Computer Engineering and Mathematics at the University of Arizona and a Director of the Error Correction Laboratory. He is an inventor of the soft error-event decoding algorithm for intersymbol interference channels with correlated noise, and the key architect of a detector/decoder for Bell Labs data storage read channel chips which were regarded as the best in industry. His pioneering work on structured low-density parity check (LDPC) error correcting codes based on combinatorial designs has enabled low-complexity iterative decoder implementations. Structured LDPC codes are today adopted in a number of communications standards and data storage systems. Dr. Vasic's work on codes on graphs, trapping sets and error floor of iterative decoding algorithms has led to decoders for the binary symmetric channel with best error-floor performance known today. He is a founder of Codelucida, a company developing advanced error correction solutions for communications and data storage. Recently, Codelucida has received numerous innovation awards including 2017 Arizona Innovation Challenge Award from Arizona Commerce Authority, 2018 I-Squared Startup of the Year from Tech Launch Arizona, and Best of Show Award for the Most Innovative Flash Memory Technology at the 2019 Flash Memory Summit, the World largest exhibition of flash memory technologies. Codelucida is a Xilinx Partner providing LDPC Codec IP cores for flash memory controllers. He is an IEEE Fellow, Fulbright Scholar, da Vinci Fellow, and a past Chair of IEEE Data Storage Technical Committee. Currently, he is in the Workforce Technical Advisory Committee within the Quantum Economic Development Consortium (QED-C), established with support from the National Institute of Standards and Technology (NIST) as part of the Federal strategy for advancing quantum information science called for by the National Quantum Initiative Act in 2018. Dr. Vasic is also a PI on a Department of Energy multi-university project led by Fermi National Laboratory to establish a Center for Superconducting Materials and Systems. He is also involved in University of Arizona Quantum Hub, a group of researchers leading effort to establish a graduate program in quantum information science and engineering at the UArizona.